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2814

BOX AFTER FINAL

Docket: 0819-0255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT Application of  
Hiroshige HIRANO et al.

Serial No.: 09/333,049

Filed: June 15, 1999

For: FERROELECTRIC MEMORY DEVICE



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Art Unit: 2814

JAN 03 2001

Examiner: Hoai Phan TECHNOLOGY CENTER 2800

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TRANSMITTAL LETTER

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Transmitted herewith is an Amendment After Final Rejection, and a Transmittal Letter in the above-identified application.

The fees have been calculated as shown below:

	Claims Remaining After Amendment		Highest Number Previously Paid For	Present Extra	Small/Large Entity Rate	Fee
Total	10	Minus	20	0	x \$9/\$18	\$ .00
Indep	1	Minus	3	0	x \$40/\$80	\$ .00
First Presentation of Multiple Dependent Claim					+ \$135/\$270	\$ .00
TOTAL						\$ .00

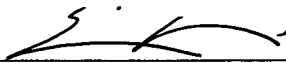
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- ☐ A check in the amount of \$ to cover the extension fee is enclosed.
- ☒ In the event applicant(s) has overlooked the need for any petition and fee for extension of time, and such extension is required, applicant(s) requests that this be considered a petition therefor and that such fee be charged to Deposit Account No. 19-2380.
- ☒ The Commissioner is hereby authorized to charge fees under 37 CFR 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c) and 1.20 (d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment, to Deposit Account No. 19-2380. A duplicate copy of this sheet is attached.

Respectfully submitted,

NIXON PEABODY LLP



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Eric J. Robinson  
Reg. No. 38,285

EJR/CTB/lfm

Attorney Docket No.: 0819-0255

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**BOX AFTER FINAL**

Attorney Docket No.: 0819-0255

**RESPONSE UNDER 37 CFR 1.116 EXPEDITED PROCEDURE  
EXAMINING GROUP 2814**

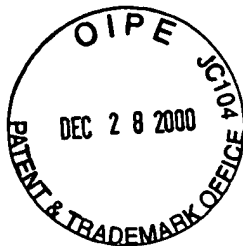
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**AMENDMENT AFTER FINAL REJECTION UNDER 37 C.F.R. §1.116**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Sir:

In response to the Office Action dated September 26, 2000, please amend the above-identified application as follows:

**IN THE CLAIMS:**

Please amend claim 1 as follows:

- sub c1  
B,
1. (Twice Amended) A ferroelectric memory device comprising:  
a ferroelectric capacitor including a top electrode, a bottom electrode and a ferroelectric film interposed between the top and bottom electrodes, the top electrode having a rectangular planar pattern;  
a memory cell transistor including first and second doped layers and a gate, the memory cell transistor controlling a voltage supplied to the top electrode of the ferroelectric capacitor;  
an interlevel dielectric film formed over the memory cell transistor and the ferroelectric capacitor; and  
a first interconnection layer formed on the interlevel dielectric film,